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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/688,989	10/17/2000	Yoshitaka TSUNASHIMA	04329.1952-01000	2408

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EXAMINER	
RAO, SHRINIVAS H	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 02/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/688,989	TSUNASHIMA ET AL.	
	Examiner	Art Unit	
	Steven H. Rao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *27,28 and 30-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *27,28 and 30-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 October 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

Applicants' amendment filed March 17, 2004 has been entered. Therefore claims 27,28,31,32 and 33 as amended by the amendment and claim 30 as previously recited are currently pending in the Application.

Claims 1-26 were previously cancelled. Claim 29 is presently cancelled.

Drawings

New corrected drawings are required in this application because for the reasons set out in the enclosed PTO-948.

The confusion about drawings arose because of two sets of drawings. The Examiner indicated In the O/A mailed June 06, 2002 that the drawings filed on October 01, 2000 (37 pages) were acceptable.

However a set of drawings dated October 17, 2000 (and not October 01, 2000) were reviewed by the drafts person on June 16, 2003 and the objections to the drawings filed on October 17, 2000 are listed in the enclosed PTO-948.

. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Claim R jections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 27,28 30-33 are rejected under 35 U.S.C. 102(b) as being anticipated by Kume et al. (U.S. Patent No. 5,188,976, herein after Kume)

With respect to claim 27, Kume describes a semiconductor device comprising :

A semiconductor substrate including a first and second region separated by an isolation element (Kume figure 7 memory and peripheral areas) , a first transistor formed on the first region of the substrate and including a first insulation film and a first gate electrode arranged in a first direction (Kume figs.7, 9, 11 transistor in memory area) and a second transistor formed on the second region of the substrate including a second insulation film and a second gate electrode (Kume transistor in the peripheral circuit area figs 7, 9,11)., wherein a sidewall of the first gate electrode is connected to a sidewall of the second gate electrode (Kume figure 15, side wall of first gate electrode 17(memory area) is connected to sidewall of second gate 17 (first peripheral area) col. 12 lines 48-61) above isolation element when viewed from a direction perpendicular to the first direction. (figs. 7,9,11, 14 #21 above isolation elements18,19,20 (which are over gate 17).

With respect to claim 28, Kume describes the a semiconductor device of claim 27 wherein the side insulator film is substantially perpendicular to a surface of said semiconductor substrate.(Kume fig. 18, 40 is perpendicular to 11).

With respect claim 30, Kume describes the a semiconductor device of claim 27 wherein at least one of said first and second gate electrodes is formed by a damascene process (Kume col. 4 lines 19-31).

With respect to claim 31, Kume describes the device of claim 33, the first insulation film is thinner than the second insulation film, the first transistor forms a logic circuit and the second transistor forms in a memory cell (Kume figs. 4 and 18).

With respect to claim 32, Kume describes a device according to claim 33, wherein top surfaces of the first and second gate electrodes layer are coplanar . (Kume fig 18) .

With respect to claim 33, Kume describes a device according to claim 27, wherein the second transistor further comprises, a poly silicon layer formed on the second insulation film formed on the substrate (Kume figs. 22 # 17 formed on layer 16) a side insulator film formed on a sidewall of the second insulation film and the side wall of poly silicon layer (Kume fig. 22 30 formed on sidewall of 16, 17), the second gate electrode is formed on the poly silicon layer (fig.22 27 and the side wall of the first gate electrode is connected to the side wall of the second gate electrode and a side wall of the poly silicon layer via the side insulator film. (Kume figures 14, 22 side wall of first gate electrode 17(memory area) is connected to sidewall of second gate 17 (first peripheral area) via insulator film 18-20 or 33,34 col. 12 lines 48-61)

Response to Arguments

Applicant's arguments filed march 24, 2004 are moot in view of the new rejection.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory

period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven H. Rao whose telephone number is (703) 3065945. The examiner can normally be reached on 8.00 to 5.00.

The fax phone numbers for the organization where this application or proceeding is assigned are (703) 7463926 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 3067722.

Steven H. Rao

Patent Examiner.

August 8, 2004